Low frequency noise in long channel amorphous In–Ga–Zn–O thin film transistors

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We investigated the low-frequency noise properties in the inverted-staggered amorphous In–Ga–Zn–O (a-IGZO) thin-film transistors (TFTs) with the silicon dioxide (SiO_2) gate dielectric. The dependence of noise level on gate area indicates that the $1/f$ noise is the dominate source and the contribution from TFT parasitic resistances can be ignored in long channel devices. The gate voltage dependent noise data closely follow the mobility fluctuation ($\Delta\mu$) model, and the Hooge's parameter (α_H) was extracted to be $\sim 1.52\times 10^{-3}$, which is much lower than the reported α_H for a-Si:H TFTs. Finally, in the comparative study, the noise level in an unannealed a-IGZO TFT was found to be higher than that in an annealed device. The present results suggest that the $1/f$ noise in our a-IGZO TFT samples is sensitive to the active layer quality (i.e., concentration of conduction band-tail and/or deep gap states). In addition, the observed low noise in a-IGZO TFT can be associated with the *s*-orbital conduction in amorphous oxide semiconductor. © *2010 American Institute of Physics*. [doi:10.1063/1.3490193]

I. INTRODUCTION

Recently, amorphous oxide semiconductor such as amorphous In–Ga–Zn–O (a-IGZO) drew much attention worldwide and there has been a considerable progress in developing the a-IGZO thin-film transistor (TFT) technology during the past few years. The most attractive feature of a-IGZO is probably the high electron mobility in amorphous state,[1–3] which potentially allows a faster TFT (Refs. 4–6) and circuits. It is explained that a high field-effect mobility is made possible by electrons drifting through the metal-*n*s (rather than the sp^3 in amorphous silicon) orbitals in a-IGZO.[1] Today, many TFTs made from a-IGZO show a good large area uniformity,[7,8] a high electron mobility,[9] visible light transparency,[1] and decent electrical stability.[10,11] These merits make them the strong candidates for replacing the hydrogenated amorphous silicon (a-Si:H) TFTs in demanding high-resolution flat-panel display[7,12] or digital imaging applications.[13–15]

Because the TFTs will be used as the active switch for addressing the pixel electrode circuit, to ensure a good system performance (especially for the image acquisition device[14]), their low frequency noise levels should be carefully examined and minimized. The properties of low frequency drain current noise in a-Si:H or polysilicon (poly-Si) TFTs were reported by many groups.[16–20] These results often reveal $1/f$ noise (also known as flicker noise) as the dominant low frequency noise source. In many cases, the noise levels are sensitive to the active layer or/and the gate insulator quality. In general, the noise levels in a-Si:H and poly-Si TFTs are higher than the levels observed in crystalline silicon metal-oxide-semiconductor field-effect transistors (MOSFETs).[17] So far similar information for a-IGZO TFTs is still very limited. Lee *et al.*[21] reported the characteristics of low-frequency $1/f$ noise in staggered a-IGZO TFTs with Al_2O_3 as gate insulator. They pointed out that the noise level can be modeled by the mobility fluctuation model with the Hooge's parameter (α_H) of 1.41, which is higher than the typical value of $\sim 10^{-2}$ for a-Si:H TFT.[16] In a subsequent study, Cho *et al.*[22] compared the noise levels of staggered a-IGZO TFTs with Al_2O_3 and Al_2O_3/a-SiN_x gate insulators. The latter (Al_2O_3/a-SiN_x) showed improvement in noise level ($\alpha_H \sim 6\times 10^{-3}$), and the excess electron-phonon scattering that originates from the remote phonon modes in Al_2O_3 was suggested to be the cause of a higher noise in a-IGZO TFT with the Al_2O_3 gate insulator.

Despite these initial results obtained for a-IGZO TFT with a high-*k* dielectric (i.e. Al_2O_3), there is a lack of information on noise in devices with the other important and/or more common gate insulator materials such as silicon dioxide (SiO_2). Moreover, to collect more pertinent noise results to the industrial technology development, a mainstream TFT structure, i.e. inverted-staggered structure[5,9] should be adopted in such investigations.

In this work, we present the detail analysis of the noise properties for inverted-staggered a-IGZO TFT with SiO_2 gate dielectric. The dependence of noise level on device area and bias voltage will be discussed. Finally, we point out the importance of thermal annealing in improving the device I-V (current-voltage) and noise properties.

II. COMMON LOW FREQUENCY NOISE SOURCES IN THIN FILM TRANSISTORS

A. Thermal noise

A resistor which is in thermal equilibrium with its surroundings shows random short-circuit current (or open-

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circuit voltage) fluctuations at its two terminals. Such noise was first measured by Johnson,[23–25] and soon after, its theoretical power spectrum density was derived by Nyquist[26] from an argument based on thermodynamics and the exchange of energy between resistive elements under thermal equilibrium. Therefore, thermal noise is also frequently referred to as Johnson noise or Nyquist noise. From microscopic point of view, thermal noise is fundamentally due to the random thermal motion of the electrons within resistive material (similar to Brownian movement).[27]

The thermal noise of a resistor R can be modeled by a parallel current source, with a noise power spectral density of

$$S_I(f) = \frac{4kT}{R}, \tag{1}$$

where S_I has the unit of amphere square per hertz, k is the Boltzmann constant, and T is the kelvin temperature. Since Eq. (1) is independent of frequency, thermal noise is categorized as white noise.[28] In c-Si MOSFET, the resistive transistor channel also exhibits thermal noise. By treating the channel as a resistor whose incremental resistance is a function of the position along channel length direction, van der Ziel[29] showed that the thermal noise in FET drain current is

$$S_I(f) = \gamma 4kTg_{ds0}, \tag{2}$$

where

$$\gamma = \frac{1 - \nu + \frac{1}{3}\nu^2}{1 - \frac{1}{2}\nu}, \tag{3}$$

$$g_{ds0} \equiv \left(\frac{\delta I_D}{\delta V_{DS}}\right)\Bigg|_{V_{DS}\sim 0} = \mu_{eff} C_{ox} \frac{W}{L}(V_{GS} - V_{th}). \tag{4}$$

In Eqs. (3) and (4), the ν is defined as

$$\nu \equiv \frac{V_{DS}}{(V_{GS} - V_{th})}, \tag{5}$$

and g_{ds0} is the channel conductance when FET drain to source voltage $(V_{DS}) \sim 0$ V (linear region); I_D is the TFT drain current; V_{GS} and V_{th} are the gate-to-source voltage and threshold voltage, respectively; W and L are TFT channel width and length, respectively; C_{ox} is the gate insulator capacitance per unit area and μ_{eff} is the field-effect mobility. It can be easily shown that, when $V_{DS} \ll (V_{GS} - V_{th})$, $\nu \sim 0$ and $\gamma = 1$. On the other hand, in saturation region, $V_{DS} = V_{GS} - V_{th}$, therefore, $\nu = 1$ and $\gamma = 2/3$. Not just in c-Si MOSFET, equation similar to Eq. (2) has also been applied to model the thermal noise in TFT (e.g., a-Si:H TFT).[18]

B. Flicker (1/f) noise

For surface conducting devices like c-Si MOSFETs or a-Si:H TFTs, flicker noise is generally the dominated low frequency noise source. This type of noise is mostly observed with a drain current noise power spectral density inversely proportional to frequency

$$S_I(f) \propto \frac{1}{f^\Gamma}, \tag{6}$$

where Γ is more or less constant (~ 1) and usually lies between 0.8 and 1.4.[27] Hence, the flicker noise is also often referred to as "$1/f$ noise."

Although the physical origins of $1/f$ noise in c-Si MOSFET (or a-Si:H TFT) have been discussed for nearly half a century, they are still obscure and under active research (to name a few: Refs. 30–33). There are two different schools of thought: number fluctuation (Δn) theory and mobility fluctuation $(\Delta \mu)$ theory. The number fluctuation theory treats the $1/f$ waveform as a superposition of a large number of relaxation processes (each with a Lorentzian power spectrum of $4\tau/(1+\omega^2\tau^2)$) with a wide spread of time constants (τ). More importantly, the distribution function of $\tau[\rho(\tau)]$ should proportional to $1/\tau[\rho(\tau) \propto 1/\tau$, i.e. the process with shorter τ is more likely to occur].[32] In year 1957, McWhorter[34] first proposed that the relaxation process could be originated from the electron random trapping/detrapping and the distribution of trapping times might arise from the tunneling of charge from the semiconductor surface to traps located in the oxide. He suspected that the oxide traps are homogeneous within a specific depth range, because the $\rho(\tau)$ is proportional to $1/\tau$ under this assumption. Christensson *et al.*[35] later pointed out such trapping/detrapping can occur near the channel/gate insulator interface and successfully extend this concept to the c-Si MOSFET. The Δn model describes the transistor drain current noise (S_{ID}) by following equation:[17]

$$S_{ID} = \frac{k^*}{f} \frac{\mu_{eff}}{C_{ox} L^2} \frac{I_D V_{DS}}{(V_{GS} - V_{th})}. \tag{7}$$

The k^* is a coefficient related to the tunneling possibility between channel and gate insulator traps

$$k^* = \frac{q^2 D_t(E_F) kT}{\ln(\tau_2/\tau_1)}, \tag{8}$$

where $D_t(E_F)$ is the active trap density in the vicinity of the Fermi level (E_F), and τ_1 and τ_2 are the lower and upper boundaries of time constants involved in the trapping/detrapping process. The drain current noise is also often represented as normalized noise, $S_{ID}/(I_D)^2$. In standard c-Si MOSFET model, the linear region drain current can be written as

$$I_D = \mu_{eff} C_{ox} \frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2\right]. \tag{9}$$

Combining Eqs. (7) and (9), we can have

$$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f} \frac{1}{C_{ox}^2 WL} \frac{1}{(V_{GS} - V_{th})} \frac{1}{[(V_{GS} - V_{th}) - \frac{1}{2}V_{DS}]} \tag{10}$$

or

$$\frac{S_{ID}}{I_D^2} = \frac{k^*}{f} \frac{1}{C_{ox}^2 WL} \frac{1}{(V_{GS} - V_{th})^2} \frac{1}{(1 - \nu/2)}, \tag{11}$$

where ν was defined in Eq. (5). From previous discussion, we have shown that when $V_{DS} \ll V_{GS} - V_{th}$ (linear region), $\nu \sim 0$; and in saturation region, $V_{DS} = V_{GS} - V_{th}$, so $\nu = 1$. The

TABLE I. Comparison of Δn and $\Delta\mu$ models in linear and saturation regions.

	McWhorter Δn model	Hooge $\Delta\mu$ model
Linear region	$\frac{S_{ID}}{I_D^2}=\frac{k^*}{f}\frac{1}{C_{ox}^2WL}\frac{1}{(V_{GS}-V_{th})^2}$	$\frac{S_{ID}}{I_D^2}=\frac{\alpha_H}{f}\frac{q}{C_{ox}WL}\frac{1}{(V_{GS}-V_{th})}$
Saturation region	$\frac{S_{ID}}{I_{D\_sat}^2}=\frac{k^*}{f}\frac{2}{C_{ox}^2WL}\frac{1}{(V_{GS}-V_{th})^2}$	$\frac{S_{ID}}{I_{D\_sat}^2}=\frac{\alpha_H}{f}\frac{2q}{C_{ox}WL}\frac{1}{(V_{GS}-V_{th})}$

same results can also be derived from gate voltage noise (or input referred noise) by assuming the power spectrum density of the fluctuation in the number of occupied traps is $1/f$ in nature.[36,37]

McWhorter's Δn theory implies that $1/f$ noise is fundamentally a surface effect. In contrast to this concept, in 1969, Hooge claimed the $1/f$ noise is not surface effect by formulating an empirical law, which appears to be representative to many observed $1/f$ noises in homogeneous samples.[38] The empirical law stated that the normalized current noise is inversely proportional to the total number of charge carriers in sample

$$\frac{S_{ID}}{I_D^2}=\frac{C}{f}=\frac{\alpha_H}{fN}, \tag{12}$$

where $C\equiv\alpha_H/N$; N is the total number of charge carriers involved in the conduction of the sample and α_H is an empirical dimensionless constant (also called Hooge's parameter). In the subsequent work, Hooge and Vandamme showed that the $1/f$ noise should originate from noise in lattice scattering, which in turn causes random mobility fluctuation.[39] Many other studies have supported this idea.[40] The α_H was originally proposed as an "universal constant" for homogeneous materials with the value of 2×10^{-3}. But it was soon be found that α_H is technology/material dependent and in c-Si MOSFET, V_{GS} dependent.[32,33] Nonetheless, α_H can still be considered as a device/material quality indicator. In a high quality c-Si or c-SiGe MOSFETs, α_H can range from 10^{-6}–10^{-4}. In a-Si:H TFTs, the α_H is reported to be $\sim10^{-2}$.[16] The α_H values in range of 5–20 have also been reported for organic TFTs.[41]

Following Rhayem,[42] we derive the $\Delta\mu$ model for c-Si MOSFET (or TFT) by starting with the total numbers of carriers in the FET channel

$$N=\frac{C_{ox}WL}{q}(V_{GS}-V_{th}). \tag{13}$$

Merge Eqs. (13) and (12), we have

$$\frac{S_{ID}}{I_D^2}=\frac{q}{C_{ox}WL}\frac{\alpha_H}{f}\frac{1}{(V_{GS}-V_{th})}. \tag{14}$$

The S_{ID} can also be rewritten as a function of I_D. In linear region, under the assumption of $V_{DS}\ll V_{GS}-V_{th}$, $I_D=\mu_{eff}C_{ox}(W/L)(V_{GS}-V_{th})V_{DS}$ and Eq. (14) becomes

$$S_{ID}=\frac{\mu_{eff}q}{L^2}\frac{\alpha_H}{f}I_DV_{DS}. \tag{15}$$

It should be notice that Eq. (15) is consistent with the results from Klaassen[43] and Vandamme's works.[44] To derive the S_{ID} in saturation region, we combine Eqs. (15) and (9) (Ref. 17)

$$S_{ID}=\frac{\alpha_H}{f}q\mu_{eff}^2C_{ox}\frac{W}{L^3}(V_{GS}-V_{th})^3\nu^2\left(1-\frac{\nu}{2}\right). \tag{16}$$

In saturation region, $\nu=1$ and therefore

$$S_{ID}=\frac{1}{2}\frac{\alpha_H}{f}q\mu_{eff}^2C_{ox}\frac{W}{L^3}(V_{GS}-V_{th})^3$$
$$=\frac{\alpha_H}{f}q\sqrt{2}\left(\frac{\mu_{eff}}{C_{ox}}\right)^{1/2}\frac{1}{W^{1/2}L^{3/2}}(I_{D\_sat})^{3/2}, \tag{17}$$

where $I_{D\_sat}[\mu_{eff}C_{ox}W/2L(V_{GS}-V_{th})^2]$ is the drain current in saturation region. Alternatively, we can obtain the normalized drain current noise for saturation region:

$$\frac{S_{ID}}{I_{D\_sat}^2}=\frac{\alpha_H}{f}q\sqrt{2}\left(\frac{\mu_{eff}}{C_{ox}}\right)^{1/2}\frac{1}{W^{1/2}L^{3/2}}(I_{D\_sat})^{-1/2}. \tag{18}$$

By substituting $(I_{D\_sat})^{-1/2}$ with the standard MOSFET equation, Eq. (18) becomes

$$\frac{S_{ID}}{I_{D\_sat}^2}=\frac{\alpha_H}{f}\frac{2q}{C_{ox}WL}\frac{1}{(V_{GS}-V_{th})}. \tag{19}$$

Table I summarizes the normalized $1/f$ noise spectral densities predicted by both Δn and $\Delta\mu$ models. It should be noticed that both models have similar mathematical forms and are both inversely proportional to the device area $[(WL)^{-1}]$. Beside the dependence of $1/f$ noise on C_{ox} (or gate insulator thickness), dependence on effective gate voltage $(V_{GS}-V_{th})$ can also be used to differentiate these two models.

Assuming that during current-voltage (I-V) measurement, a constant voltage maintains the pure dc level; the observed $1/f$ noise in current can only arise from the fluctuation of sample resistance. Since the resistance depends on the density and mobility of the charge carriers, it is naturally to conclude that the $1/f$ noise is due to charge number or mobility fluctuation. Perhaps the difficulty in achieving a conclusive physical origin for $1/f$ noise is that numerous experimental evidences support (or against) either theory. Experimental results collected for homogeneous samples usually follow the $\Delta\mu$ model.[38,39] In MOSFET, n-MOS $1/f$ noise obeys the Δn model while the $\Delta\mu$ model explains p-MOS $1/f$ noise better.[30,32,33] The $1/f$ noises in a-Si:H TFT generally follow the $\Delta\mu$ model[16] but a trend towards Δn

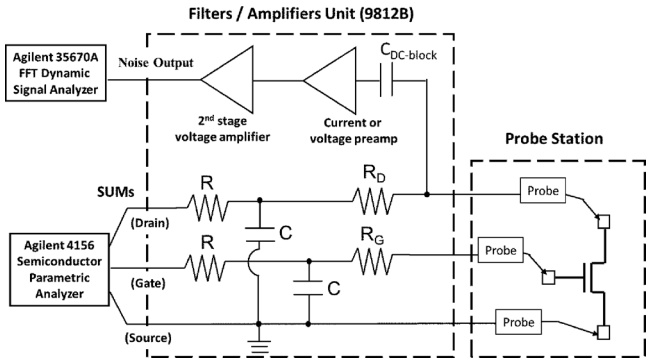

FIG. 1. Circuit diagram of the experimental setup used for measuring the TFT drain current noise. The filter/amplifier unit is also known as 9812B noise analyzer. (Adapted from Ref. 46). Device is placed inside the light-tight probe station, which also serves as a Faraday cage for electrical shielding.

mode was also found in short channel device ($L < 5\ \mu m$).[17] It is possible that both mechanisms co-exist simultaneously in the device: In a long channel TFT, the excess bulk defects cause the $\Delta\mu$ $1/f$ noise to be the predominant one. On the other hand, in a short channel device, the impact of interface trapping/detrapping can become more significant.

III. EXPERIMENTAL

The TFTs used in this study have the common gate, inverted-staggered structures (inset of Fig. 3 is the cross-sectional view). A detail discussion of the processing steps was provided elsewhere.[9] The device consists of a 20 nm thick a-IGZO channel layer and a 100 nm thick thermal SiO_2 gate insulator layer. The heavily doped (n^{++}) silicon (Si) substrate also serves as the gate electrode. After the a-IGZO active island was being patterned, the device is thermally annealed at 300 °C for 20 min in air. Finally, the gold/titanium (Au/Ti) stacked layer (40/5 nm thick) is deposited; and the S/D electrodes are patterned by the lift-off technique.

Figure 1 illustrates the experimental setup that is used to measure the a-IGZO TFT drain current noise power spectrum under different bias conditions. The device-under-test (DUT) is voltage biased, and its current noise is analyzed. The core of this system is the filter/amplifier unit (also known as 9812B Noise Analyzer made by ProPlus Design Solution, Inc.). The unit contains a high quality RC low-pass filters (cut-off frequency of 0.1 Hz is used) for removing the source-measure unit (SMU) noise from semiconductor parametric analyzer (Agilent 4156C). Thus, the DUT bias voltages are very close to the pure dc signals and "noise free." The output load resistor (R_D) and input series resistor (R_G) are used for the purpose of impedance matching between the DUT and internal low noise amplifiers. The DUT can be either two or three terminals. For measuring resistor noise, the gate SMU is not used. For TFT noise measurement, the R_G is short ($0\ \Omega$) due to the high gate impedance. The computer program automatically selects optimal R_D according the bias condition and the selection of low noise amplifier.[45] For reference, the typical R_D value used in this study is 33 or 100 $K\Omega$. The dc block capacitor (C_{dc_block}) serves as ac input coupling capacitance of low noise amplifiers. The amplifiers pick up and enhanced the ac noise signal form DUT. There are two amplifiers available in 9812B, voltage and current amplifiers. Each has a working frequency range of 1 MHz and they are battery operated. The voltage amplifier has a voltage gain of 20; and the current amplifier has a feedback resistor (R_a) of 40 $K\Omega$. Both amplifiers are followed by a 2nd stage amplifier with a voltage gain of 25. Therefore, the 9812B system can provide an overall voltage gain of 500 or current-to-voltage gain of 1 mV/1 nA on noise signal.[46] The selection between these two amplifiers usually depends on the device output impedance. For example, when TFT is bias in linear region, the output impedance is low and the voltage amplifier should be used. On the other hand, when the TFT is operated in saturation region with a high output impedance; the current amplifier should be chosen.

The noise measurement flow can be broken down into two stages. During the first stage, the computer controls the Agilent 4156C to establish bias on DUT (e.g. TFT or resistor). Multiple iterations are applied to make sure the DUT bias signals are stable and equal to the programmed value (<2% error). The settling time usually takes at least four low-pass RC time constants, which correspond to ~40 s. During the second stage, the low noise amplifier circuit is engaged. The amplified TFT drain current noise signals are than collected by Agilent 35670A fast Fourier transform (FFT) dynamic signal analyzer. To have the frequency domain noise spectrum, the 35670A applies FFT on the data collected in time domain. The entire frequency range is divided into several subbands by 35670A and the final noise spectrum is composed from data collected at each band. Progressive increases in average number are applied: data collected from low frequency band (0.4–25 Hz) is average from ten measurements, while high frequency band (200–12.8 KHz) is average from more than forty measurements.

Since the final noise output contains additional noise signals from load resistor (i.e. R_D) and amplifiers, the computer program performs a data correction routine on raw data to extract the accurate noise signal of interest. To verify the overall system performance, we measured the thermal noise spectrums from high quality metal film resistors ranging from 500–1 $M\Omega$.[47] From this data, we estimated the noise detection limit for our system to be $\sim 10^{-25}$ A^2/Hz, corresponding to $R < 100$ $K\Omega$. In addition, the measurement data are very close to the theoretical values, supporting that the data correction routine is functioning properly in the present experimental set up.

IV. EXPERIMENTAL RESULTS AND DISCUSSION

A. Electrical properties of the a-IGZO TFT

The transistor electrical properties were measured by a PC controlled Agilent 4156C semiconductor parametric analyzer. Figure 2 illustrates the linear region ($V_{DS}=0.1$ V) transfer characteristics of the common gate, rf sputter a-IGZO TFT ($W/L=180\ \mu m/30\ \mu m$). We extracted V_{th} and μ_{eff} based on the standard MOSFET Eq. (9). The straight lines in Fig. 2 represent the best linear fits of Eq. (9) between 90% to 10% of the maximum I_D (at $V_{GS}=20$ V), and the V_{th} and μ_{eff} are extracted to be 2.07 V and 12.8 cm^2/V s, re-

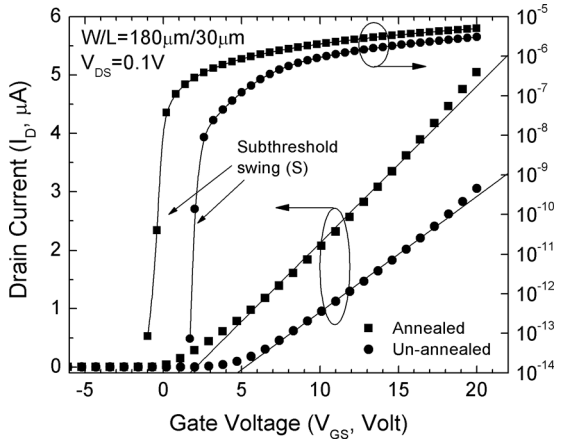

FIG. 2. Linear region transfer properties of rf sputter a-IGZO TFTs in semi-log (right *Y*-axis) and linear (left *Y*-axis) plots. Symbol (■) and (●) are experimental data for annealed and unannealed devices, respectively.

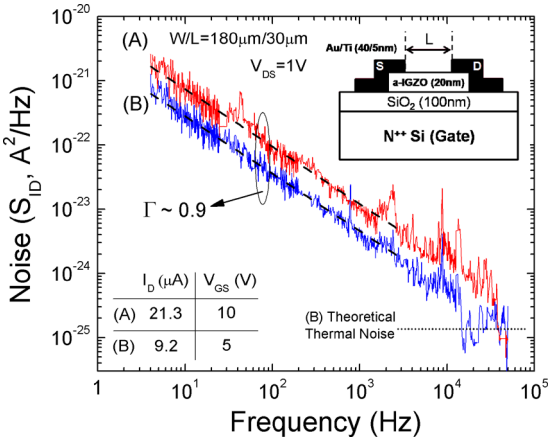

FIG. 3. (Color online) Example of a-IGZO TFT drain current noise spectrum (S_{ID}). Two linear region noise data are shown (V_{DS}=1 V). Data A (red) and B (blue) are measured under V_{GS} of 10 V and 5 V, respectively. (Inset) The cross section view of the common gate, rf sputter a-IGZO TFT used in measurements. (Dotted line) Thermal noise floor of condition B estimated from the theoretical model (2).

spectively. (The properties of the unannealed device will be discussed in Sec. IV E.) The subthreshold swing (S) was also extracted from subthreshold region data at the maximum slope point (Fig. 2), using equation[48]

$$S = \left[\frac{\delta \log(I_D)}{\delta V_{GS}}\right]^{-1}. \tag{20}$$

Table II summarizes all the TFT key parameters extracted from experimental data. The observed high μ_{eff} and low S of the annealed device indicate the TFT active layer and a-IGZO/SiO_2 interface qualities are well controlled during device fabrication; and it is suitable for the subsequent noise measurements and analysis.

B. Example of the a-IGZO TFT drain current noise spectrum

Figure 3 shows two examples of S_{ID} spectrums collected for the annealed a-IGZO TFT. (In Sec. IV, unless otherwise specify, all noise spectrum data are collected from this type of TFT.) It is clear that when the device is operating under a higher I_D (by increasing V_{GS}), its noise level also increases. The noise spectrums have a $1/f^{\Gamma}$ shape, which almost extends the entire measurement range (4–10 KHz). The Γ of the spectrums in Fig. 3 is 0.9, which is determined by the best linear fits (dashed lines) of Eq. (6) to experimental data between 6~500 Hz. In fact, throughout this study, the Γ values we extracted are between 0.89 and 1.05 (with an average of 0.95, standard deviation of 0.052). This fits the general description of $1/f$ noise as described in literature[27,32] and suggests the $1/f$ noise is the dominated noise source in our a-IGZO TFTs.

TABLE II. Electrical properties of rf sputter a-IGZO TFTs.

Device	μ_{eff} (cm^2/V s)	V_{th} (V)	S (V/dec)
Annealed	12.8	2.07	0.15
Unannealed	9.54	5.21	0.14

Data (B) in Fig. 3 shows a small "flat" section in the high frequency range (>10 KHz). This part of spectrum is not very clear because it is approaching the detection limit of our setup. Nonetheless, the measured power spectrum density is close to the theoretical thermal noise floor predicted by Eq. (2). In most of the measurements, such as data (A), the flicker noise dominates the S_{ID} spectrum. Since this is the noise source that usually effects the most on circuit performance,[15] we focus on the low frequency (f<1 KHz) $1/f$ noise in a-IGZO TFT for the rest of this study.

C. Noise as a function of channel area

To further verify the nature of low frequency noise in a-IGZO TFTs, the dependence of noise on TFT channel area is investigated. The low frequency noise spectrums were measured from a set of devices with channel area ranging from 150 to 15 000 μm^2 (Table III). Since these devices have different L, W, and small variation in V_{th}, the normalized measurement conditions listed in Table III were used to properly extract noise spectrums. For measuring TFTs with different W, we control the drain currents (I_D) so that the surface current density ($\kappa = I_D/W$) is kept as a constant of 0.167 $\mu A/\mu m$. For measuring TFTs with different L, we control the drain-to-source voltage (V_{DS}) so that the electric field along the channel ($E = V_{DS}/L$) is kept as a constant of 0.02 $V/\mu m$. These values are chosen to ensure that all devices are in linear region of operation during the noise measurement and the signal strengths are well above the detection limit. The concept of the normalization can be better understood by defining the a-IGZO channel sheet resistant (R_{S_IGZO}) as

$$R_{S\_IGZO} \equiv \left(\frac{V_{DS}}{I_D}\right)\left(\frac{W}{L}\right) = \frac{E}{\kappa}. \tag{21}$$

Therefore, by maintaining the E and κ as constant, our normalized conditions give the same R_{S_IGZO} of 1.2×10^5 $\Omega/\square$ for all TFTs. By substituting the linear-region

TABLE III. Normalized measurement conditions for studying the channel area dependent noise properties. [For all devices: Surface current density ($\kappa = I_D/W$) is 0.167 $\mu A/\mu m$. Electric field along the channel ($E = V_{DS}/L$) is 0.02 $V/\mu m$.]

	TFT dimensions			Measurement conditions		
Device No.	W (μm)	L (μm)	Area (μm^2)	V_{DS} (V)	I_D (A)	R_{S_IGZO} ($\Omega/\square$)
1	300	50	15 000	1	5×10^{-5}	1.2×10^5
2	180	60	10 800	1.2	3×10^{-5}	
3		30	5 400	0.6		
4		10	1 800	0.2		
5	60	10	600	0.2	1×10^{-5}	
6	30	5	150	0.1	5×10^{-6}	

($V_{DS} \ll V_{GS} - V_{th}$) TFT drain current Eq. (9) into Eq. (21), R_{S_IGZO} can also be expressed as

$$R_{S\_IGZO} = [\mu_{eff} C_{ox}(V_{GS} - V_{th})]^{-1}. \quad (22)$$

Combine Eqs. (13) and (22), we can then express the total number of electrons (N) in the TFT channel in terms of R_{S_IGZO} by

$$N = \frac{W \times L}{q\mu_{eff} R_{S\_IGZO}}. \quad (23)$$

Equation (23) suggests that the N is directly proportional to the TFT channel area in our experiments.

Figure 4(a) illustrates the examples of noise measurement results. To minimize the error during noise data extraction, we first perform the best fits of the normalized noise spectrums to Eq. (12) or in its logarithmic form

$$\log\left(\frac{S_{ID}}{I_D^2}\right) = \log C - \log f \quad (24)$$

from 6 to 500 Hz. This approach is valid because as we have pointed out in Sec. IV B, all of our noise spectrums have the slopes very close to $1/f$. The dashed lines in Figure 4(a) represent such fits and the values of noise prefactor C can be extracted from the *Y*-intercepts. It should be noticed that the prefactor C can completely represent the entire spectrum and the $S_{ID}/(I_D)^2$ value can be calculated by Eq. (12) or (24) at any frequency point of interest. The $S_{ID}/(I_D)^2$ values at 30 Hz for different TFTs are then estimated.

As shown in Fig. 4(b), the $S_{ID}/(I_D)^2$ is inversely proportional to the channel area ($W \times L$); the slope in a dual-log plot is very close to -1. This property further confirms that the observed low frequency noise in a-IGZO TFT is flicker noise in nature and the contribution from TFT parasitic resistances can be ignored.[33] However, since both Δn and $\Delta\mu$ theories predict the same $S_{ID}/(I_D)^2$ dependence on area (Table I), to discriminate between these two models, the $1/f$ noise must be studied as a function of gate voltage. This is the topic of Sec. IV D.

If the $\Delta\mu$ model (12) is valid for our a-IGZO TFTs, we may extract the α_H by following the methodology from Hooge.[38] In Fig. 5, the noise prefactors (C) for TFTs with different areas are plotted as a function of N, which is calculated by Eq. (23), in a dual-log scale. [The μ_{eff} of 12.8 $cm^2/V\,s$ (extracted from TFT no. 3) is used for N calculation.] Hooge's model states that the C should be inversely proportional to N (Ref. 38)

$$C = \frac{\alpha_H}{N}. \quad (25)$$

As shown in Fig. 5, our experimental data agree fairly well to the model and from the suggested best fit of experimental data to Eq. (25), the α_H is determined to be 1.35×10^{-3}. [α_H

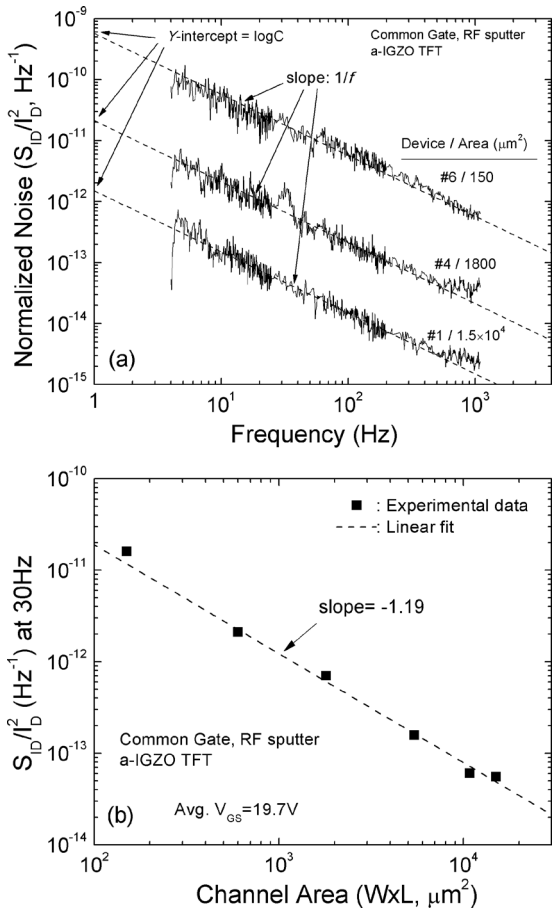

FIG. 4. (a) Examples of the normalized noise spectrums collected for three TFTs with different channel areas (150, 1800, and 1.5×10^4 μm^2). Dashed lines are the best linear fits to Eq. (24). (b) Normalized a-IGZO TFT drain current noise [$S_{ID}/(I_D)^2$] vs channel area. Data points (■) are sampled at 30 Hz. Dashed line is the best linear fit to the experimental data.

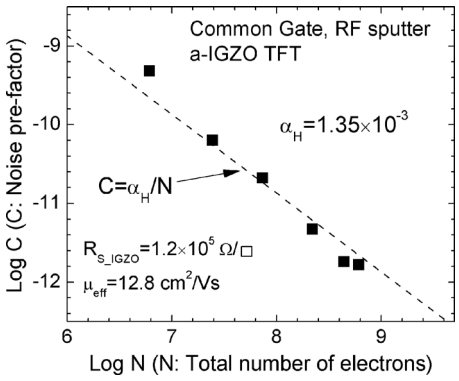

FIG. 5. Illustration of α_H extraction based on area-dependent noise data. The total carrier numbers in TFT channel (N) are calculated by Eq. (23) and are proportional to channel area. Noise prefactors C are numerically extracted from experimental noise spectrums as illustrated in Fig. 4(a). Symbol: experimental data; dashed line: suggested best fit to the Hooge model (25).

is calculated from the *Y*-intercept of the dashed line, which is not shown in Fig. 5.]

D. Noise as a function of gate voltage

The dependence of TFT drain current noise on gate voltage was studied. The noise spectrums of a-IGZO TFT were measured in both linear (V_{DS}=1 V) and saturation (V_{DS}=12 V) regions. In order to extract the noise prefactors C and $S_{ID}/(I_D)^2$ values, we followed the same methodology as described in Sec. IV C: the C values are first determined by the best linear fits of Eq. (24) from the normalized noise spectrums between 6–500 Hz. The $S_{ID}/(I_D)^2$ values (e.g., at 30 Hz) can then be calculated. Figures 6 and 7 illustrate that the normalized drain current noise (S_{ID}/I_D^2) of our a-IGZO TFT has the power law dependence with $V_{GS}-V_{th}$. The power law coefficient is extracted to be between −1.1 and −1.2, which is closed to the prediction of mobility fluctuation ($\Delta\mu$) model (i.e. slope=−1, Table I). A similar trend has also been observed for the a-Si:H TFT sample (Fig. 6), which was fabricated using an industrial standard

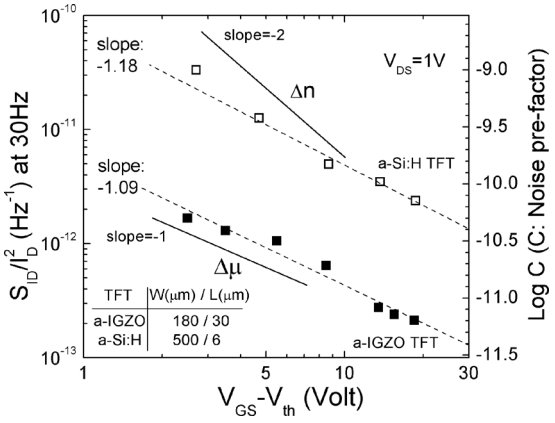

FIG. 6. Linear region (V_{DS}=1 V) $S_{ID}/(I_D)^2$ (at 30 Hz) and noise prefactor C as a function of V_{GS}-V_{th}. Solid (■) and open symbols (□) are experimental data for a-IGZO and a-Si:H TFTs, respectively. Dashed line: linear fit to the experimental data. Solid lines with slope of −2 and −1 are also provided for the aid of eye.

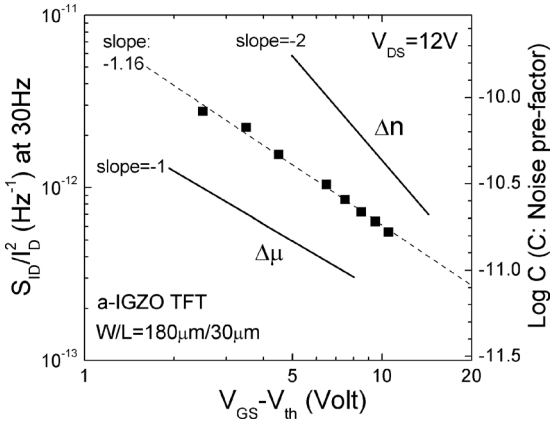

FIG. 7. Saturation region (V_{DS}=12 V) $S_{ID}/(I_D)^2$ (at 30 Hz) and prefactor C as a function of $V_{GS}-V_{th}$. Symbols: experimental data; dashed line: linear fit to the experimental data.

process.[49,50] We further extracted the α_H from the linear region noise data. By rearranging Eq. (14), the α_H can be calculated by

$$\alpha_H = \left(\frac{S_{ID}}{I_D^2}\right)\frac{C_{ox}WLf}{q}(V_{GS}-V_{th}). \tag{26}$$

As shown in Fig. 8, the α_H is independent of $V_{GS}-V_{th}$ for a-IGZO TFT (and also for a-Si:H TFT). This property strongly suggests that the $1/f$ noises in both a-IGZO and a-Si:H TFTs follow the $\Delta\mu$ model. In addition, the α_H has an average value of 1.52×10^{-3} for a-IGZO TFT, which is consistent with the value extracted from area dependent noise data ($\alpha_H \cong 1.35\times10^{-3}$, Fig. 5). As a comparison, the average α_H for our a-Si:H TFT sample ($\cong 5.32\times10^{-3}$) is about four times higher than that of a-IGZO TFT. In order to verify our extraction results, Fig. 9 demonstrates the use of Hooge $\Delta\mu$ model in simulating the a-IGZO TFT S_{ID}. Just like what has been illustrated in Fig. 3, we first perform the best linear fits of Eq. (6) [note: not Eq. (24)] from the noise spectrums between 6–500 Hz. The experimental S_{ID} values shown in Fig. 9 are then extracted from these fits at 30 Hz. Equations (15) and (17) are used to calculate the simulated S_{ID} values

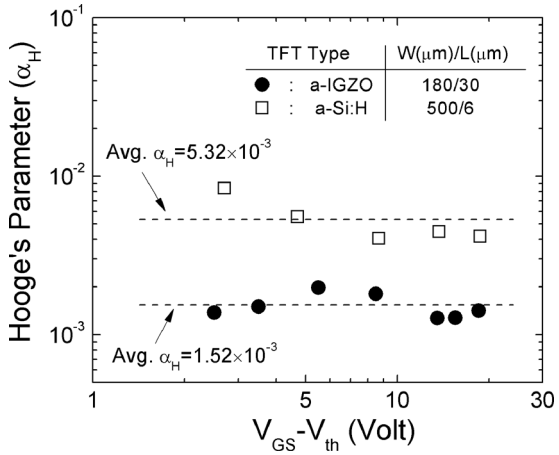

FIG. 8. Hooge's parameters (α_H) vs $V_{GS}-V_{th}$. α_H values are extracted from the linear region noise data (V_{DS}=1 V) based on Eq. (26). Symbols (●) and (□) are α_H values for a-IGZO and a-Si:H TFTs, respectively. Dashed lines indicate the average α_H values.

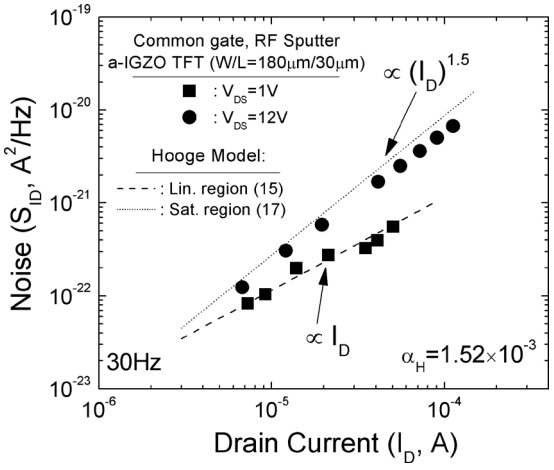

FIG. 9. Drain current noise power density (S_{ID}, sampling at 30 Hz) of the a-IGZO TFT as a function of drain current (I_D). Symbols (■, linear region) and (●, saturation region) are experimental data. Dashed and dotted lines are calculated values based on Hooge $\Delta\mu$ model.

(dashed and dotted lines). The α_H, μ_{eff}, C_{ox}, L, and W used in the calculations are 1.52×10^{-3}, 12.8 $cm^2/V\,s$, 3.453×10^{-8} F/cm^2, 30 μm, and 180 μm, respectively. The experimental data closely follow the trend ($S_{ID}\propto I_D$) simulated by the linear region Eq. (15). In addition, the saturation region noise also shows the $(I_D)^{1.5}$ law, as predicted by Eq. (17).

The α_H is frequently used as a figure of merit for the comparison of different device technologies and it is usually lower for a higher electronic quality material.[32] Figure 10 shows the reported α_H values for different TFT technologies. The data of crystalline silicon resistor are also included as reference. Clearly, the modern IC-graded resistor has the lowest reported α_H ($\sim10^{-6}$). Depending more on sample quality and preparation, α_H for bulk silicon resistors can have a wider distribution and be as high as 4×10^{-4}.[32] Our present experimental result obtained for a-IGZO TFT show better noise performance than a-Si:H TFTs ($3\times10^{-3}<\alpha_H<1.2\times10^{-2}$),[15,16,18] organic TFTs ($10^{-2}<\alpha_H<10^{2}$),[41,51] and ZnO nanowire TFT ($\alpha_H\sim6\times10^{-3}$).[52,53] As a matter of fact,

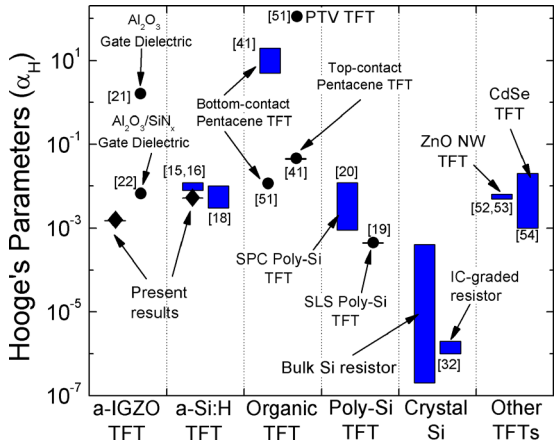

FIG. 10. (Color online) Hooge's parameter (α_H) extracted from the $1/f$ noise measurement for various TFT technologies and crystalline silicon (data from Refs. 15, 16, 18–22, 32, 41, and 51–54, which are also indicated in the figure).

its performance is more on a par with technologies like solid-phase crystallization poly-Si TFT (Ref. 20) or CdSe TFT.[54] In amorphous semiconductor TFTs, the α_H is thought to be fully, or at least partially, linked to the bulk defects.[17] In a-IGZO, the conduction band minimum (CBM) is composed of metal *s*-orbitals (primarily the In 5*s*-orbitals).[1] Due to the symmetrical nature of the *s*-orbital, such CBM is less distorted than CBM composed of sp^3 orbital in amorphous phase. Therefore, our experimental data can be explained by a lower concentrations of conduction-band tail and/or deep gap states observed in a-IGZO in comparison to other semiconductor materials (e.g. a-Si:H). Present study is in full agreement with the electronic structure (density of states) derived from photofield-effect analysis,[55] numerical simulation,[56] and others.[57] Finally, the present results also suggest the SiO_2 to be a better gate dielectric choice for a-IGZO TFTs than a high-*k* dielectric (i.e. Al_2O_3 or Al_2O_3/SiN_x) in terms of noise properties. Combining the fact that our TFT has a low subthreshold swing of 150 mV/dec, we believe that the impacts of the a-IGZO/SiO_2 interface defects or gate dielectric phonon modes on noise are small[22] and the noise data collected in this work should have a strong correlation with the a-IGZO bulk electronic properties.

E. The impact of thermal annealing on thin film transistor noise level

It is well known that the proper thermal annealing can significantly improve the a-IGZO TFT performance.[11] Hosono *et al.*[58] showed experimentally that the thermal annealing can reduce the a-IGZO optical absorption tail, improve Hall mobility, and TFT electrical properties. Based on these observations, they suggested a plausible structural relaxation, which could enhance the overlap among the In 5*s*-orbitals and lower the conduction band-tail states, induced by thermal annealing. Since the noise properties we have discussed so far are all based on TFTs that have been through the thermal annealing step, the above discussion raises a general interest in studying the noise level in the "unannealed" TFT as well.

We conduct a comparative study of $1/f$ noise in a-IGZO TFTs with and without thermal annealing step. The linear region transfer properties and key parameters for these two types of TFTs are provided in Fig. 2 and Table II, respectively. Compared to the annealed TFT, the unannealed TFT has a lower μ_{eff} (9.54 $cm^2/V\,s$) and a higher V_{th} (5.21 V). Although both TFTs have similar S values ($\sim$150 mV/dec), the unannealed TFT drain current is less responsive to gate voltage near the on-set of on-region (i.e. Figure 2, $V_{GS}=3\sim5$ V). Likewise, in a recent report on 2D numerical simulation of the a-IGZO TFT electrical properties,[56] the transfer properties were also found to be less responsive to V_{GS} when a higher conduction band-tail slope (E_a) value was used during simulation.

We collected the noise spectrum for these two types of TFTs for the same I_D of 20 μA and V_{DS} of 1 V (linear region). As shown in Fig. 11, the $S_{ID}/(I_D)^2$ of unannealed TFT is higher than that of the annealed counterpart. It should

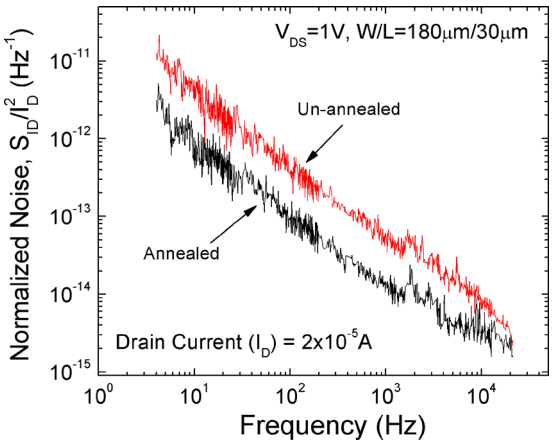

FIG. 11. (Color online) Normalized noise spectrums collected from annealed (black) and unannealed (red) rf sputter a-IGZO TFTs.

be noticed that the high $S_{ID}/(I_D)^2$ in the unannealed TFT is not due to its low mobility (or drain current), since both data are measured at the same I_D. If the previous assumption that our noise results are being dominated by the bulk defects is true, then the elevated noise level observed for the unannealed a-IGZO TFT seems to be best explained by a higher concentration of conduction band-tail and/or deep gap states in the as-deposited a-IGZO film. Therefore, the thermal annealing is a critical step in making a high performance a-IGZO TFT with the reduced conduction band-tail slope and reduced defect density that affects the electron transport. This result is consistent with Hosono *et al.*'s studies.[59] Finally, we demonstrate that the a-IGZO TFT $1/f$ noise is not only an electrical property that is important for circuit design, but may also be used as a sensitive diagnostic tool to qualify the electrical quality of semiconductor material to be used as channel layer in TFTs.

V. CONCLUSION

The low frequency $1/f$ noise properties of a-IGZO TFT were studied. The TFT noise is found to be inversely proportional to the channel area and may limit the minimum TFT size to be used in detector circuit design. By studying the $1/f$ noise as a function of gate voltage, we determined that the $1/f$ noise in a-IGZO TFT follows the Hooge's mobility fluctuation model. The model is able to well predict the linear and saturation drain current noises. Compared to a-Si:H TFT, the a-IGZO TFT has a lower noise level in nature (lower Hooge's parameter) which is very attractive to low-noise applications such as large area medical imager or detector. The $1/f$ noise is also sensitive to the a-IGZO channel/interface properties and may be used as a diagnostic tool for device quality control. It appears from this study that the silicon dioxide is suitable gate insulator for a-IGZO TFTs.

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